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29. (Amended) A semiconductor device comprising:

first and second memory cell means for storing data, the first and second memory cell means including source/drain regions; and

connecting means for electrically connecting the first and second memory cell means, the connecting means having a resistance lower than that of the source/drain regions.

Remarks

Applicant has amended claims 17, 26 and 29 to address minor informalities and clarify the claim language. No new matter has been entered. Claims 1-29 are currently pending. In view of the above, examination on the merits is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the present amendment. The attached page is captioned "Version with markings to show changes made."

Respectfully submitted,

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Version With Markings to Show Changes Made

Claims 17, 26 and 29 have been amended as follows:

17. (Amended) The semiconductor device according to <u>claim</u> [any one of claims] 13, wherein at least one part of the connecting area has almost the same impurity depth and almost the same impurity concentration of one of a source/drain area and an off-set area of MOS transistor forming a surrounding circuit of the first and second memory cell areas.

26. (Amended) A semiconductor device comprising:

first and second field effect transistors, each having source/drain regions; and a conducting region connecting a source/drain of the first field effect transistor to a source/drain of the second field effect transistor, the conducting region having a lower resistance than at least one of the source/drain regions.

29. (Amended) A semiconductor device comprising:

first and second memory cell means for storing data, the first and second memory cell means including source/drain regions; and

connecting means for electrically connecting the first and second memory cell means, the connecting means having a resistance lower than that of the source/drain regions.